

# Frequency Timing Generator for Peripherals

9FGP205

**Recommended Application:**

Peripheral Clock for Intel Servers with Wake-On-Lan support

**Output Features:**

- 1 - 0.7V current-mode differential CPU output
- 6 - 50MHz RMII outputs
- 2 - 125MHz RGMII outputs
- 1 - 0.7V current-mode differential DOT 96MHz output
- 1 - 33.33MHz output
- 1 - 32.768KHz output
- 2 - 25MHz REF outputs

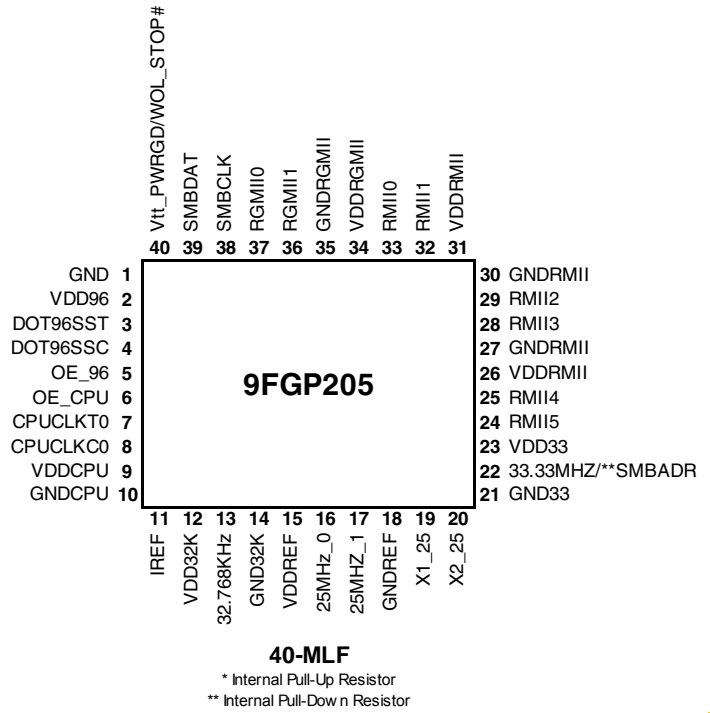
**Key Specifications:**

- Exact synthesis on CPU, RGMII, RMII & 33.33MHz clocks
- +/- 100ppm frequency accuracy on other clocks

**Features/Benefits:**

- Selectable SMBus Address - D0/D1 or C0/C1
- Spread Spectrum capability on CPU and DOT 96MHz clocks
- SMBus Control:
  - M/N and spread programming on CPU and DOT 96MHz clocks via SMBus
  - Differential outputs can be disabled via pins or SMBus

**Pin Configuration**



**Functionality**

CPU FS2	CPU FS1	CPU FS0	CPUCLK	DOT96SS	33.33	RMII	RGMII	25	32.768
Byte0 Bit2	Byte0 Bit1	Byte0 Bit0	MHz	MHz	MHz	MHz	MHz	MHz	KHz
0	0	0	266.67	96.00	33.33	50.00	125.00	25.00	32.768
0	0	1	133.33	96.00	33.33	50.00	125.00	25.00	32.768
0	1	0	200.00	96.00	33.33	50.00	125.00	25.00	32.768
0	1	1	166.67	96.00	33.33	50.00	125.00	25.00	32.768
1	0	0	333.33	96.00	33.33	50.00	125.00	25.00	32.768
1	0	1	100.00	96.00	33.33	50.00	125.00	25.00	32.768
1	1	0	400.00	96.00	33.33	50.00	125.00	25.00	32.768
1	1	1	Reserved	96.00	33.33	50.00	125.00	25.00	32.768

Power up default is highlighted.

**SMBus Address Selection**

SMBADR	
SMBADR = 0	SMBADR = 1
D0/D1	C0/C1

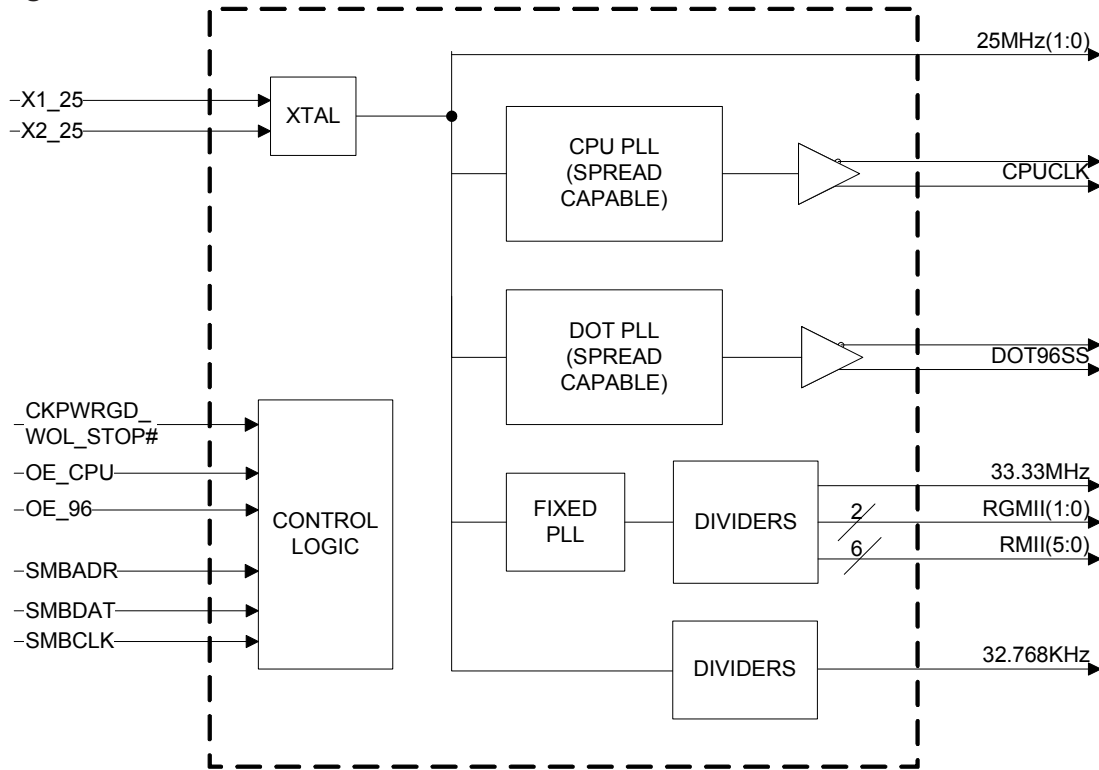
## Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	PWR	Ground pin.
2	VDD96	PWR	Power pin for the DOT96 clocks, nominal 3.3V
3	DOT96SST	OUT	True clock of differential pair for 96.00MHz spread spectrum capable DOT clock. These are current mode outputs. External resistors are required for voltage bias.
4	DOT96SSC	OUT	Complementary clock of differential pair for 96.00MHz spread spectrum capable DOT clock. These are current mode outputs. External resistors are required for voltage bias.
5	OE_96	IN	Active high input for enabling 96Hz outputs. 1 = enable output(s), 0 = tri-state output(s)
6	OE_CPU	IN	Active high input for enabling CPU DIFF pairs. 1 = enable output(s), 0 = tri-state output(s)
7	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
8	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
9	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
10	GNDCPU	PWR	Ground pin for the CPU outputs
11	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
12	VDD32K	PWR	Power pin for the 32.768KHz outputs, nominal 3.3V
13	32.768KHz	OUT	32.768KHz clock output
14	GND32K	PWR	Ground pin for the 32.768KHz outputs
15	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
16	25MHz_0	OUT	25MHz clock output, 3.3V
17	25MHz_1	OUT	25MHz clock output, 3.3V
18	GNDREF	PWR	Ground pin for the REF outputs.
19	X1_25	IN	Crystal input, Nominally 25.00MHz.
20	X2_25	OUT	Crystal output, Nominally 25.00MHz.
21	GND33	PWR	Ground pin for the 33.33MHz outputs
22	33.33MHZ/**SMBADR	I/O	33.33MHz clock output / SMBus address select bit.
23	VDD33	PWR	Power pin for the 33.33MHz outputs, nominal 3.3V
24	RMII5	OUT	3.3V 50MHz RMII clock output
25	RMII4	OUT	3.3V 50MHz RMII clock output
26	VDDRMII	PWR	3.3V power pin for the RMII clocks.
27	GNDRMII	PWR	Ground pin for the RMII outputs
28	RMII3	OUT	3.3V 50MHz RMII clock output
29	RMII2	OUT	3.3V 50MHz RMII clock output
30	GNDRMII	PWR	Ground pin for the RMII outputs
31	VDDRMII	PWR	3.3V power pin for the RMII clocks.
32	RMII1	OUT	3.3V 50MHz RMII clock output
33	RMII0	OUT	3.3V 50MHz RMII clock output
34	VDDRGMII	PWR	3.3V power pin for the RGMII clocks and PLL
35	GNDRGMII	PWR	Ground pin for the RGMII outputs
36	RGMII1	OUT	3.3V 125MHz RGMII clock output
37	RGMII0	OUT	3.3V 125MHz RGMII clock output
38	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
39	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
40	CKPWRGD_WOL_STOP#	IN	Notifies clock to sample latched inputs on first low to high transition. After first power up, a low stops all outputs except those designated to run in power down mode (WOL_STOP# mode)

## General Description

The **9FGP205** is a peripheral clock for Intel Servers. It is driven with a 25MHz crystal and generates a variety of clocks, including 125MHz RGMII. An SMBus interface allows full control of the device.

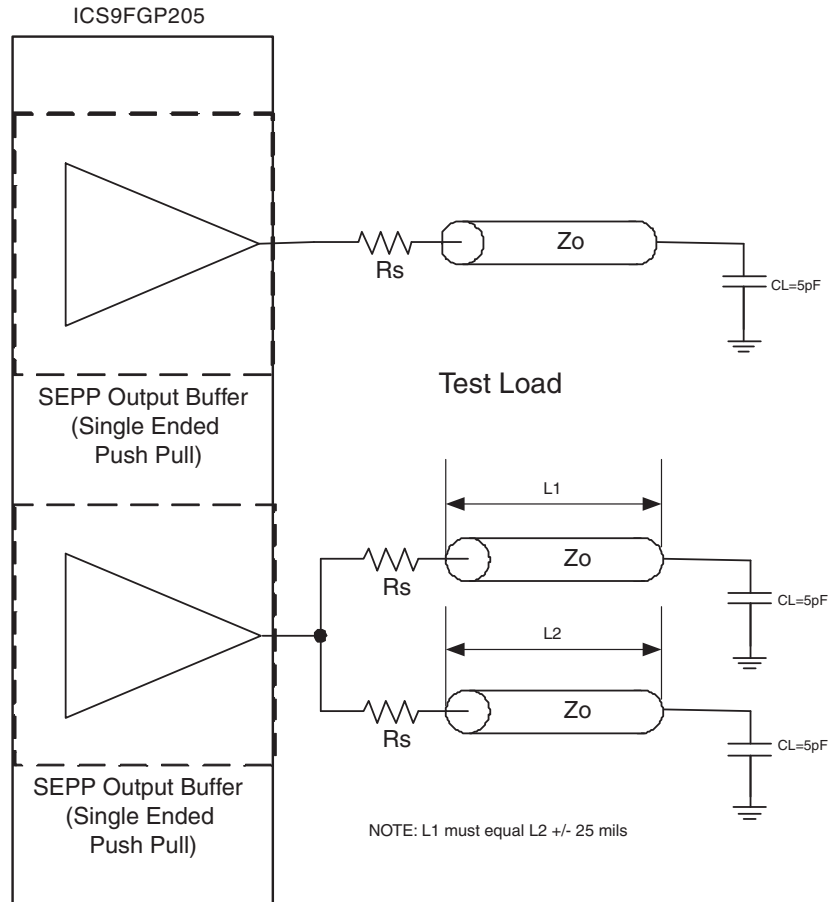
## Block Diagram



## Power Supply Pins

Pin Number		Description
VDD	GND	
9	10	CPUCLK output and PLL
2	1	DOT96SS output and PLL
34	35	125 MHz RGMII outputs and PLL
26,31	27,30	50 MHz RMII outputs
23	21	33.33MHz output
12	14	32.768KHz output
15	18	XTAL, REF outputs

Note: All VDD should be connected to a common power rail with proper filtering and decoupling. Pins 2, 9 and 34 should be treated as analog pins for decoupling purposes.



Drive Strength for all the single-ended outputs can be controlled by the SMBus Bytes 4 and 5 as shown in the Default Drive Strength Table.

**Default Drive Strength Table**

	Default Drive	Optional Drive
RGMII	1 Load	NA
RMII	1 Load	2 Loads
33.33MHz	2 Loads	1 Load
25Mhz	2 Loads	1 Load
32.768KHz	2 Loads	1 Load

**Series Termination Resistor Values EXCEPT RGMII**

Output Drive Strength	Series Resistor (Rs) for driving 1 Load	Series Resistor (Rs) for driving 2 Loads
1 Load	22 ohms	N/A
2 Loads	33 ohms	8.2 ohms

Note: All values are for Zo = 50Ω

**Series Termination Resistor Values - RGMII**

Output Drive Strength	Series Resistor (Rs) for driving 1 Load	Series Resistor (Rs) for driving 2 Loads
1 Load	27 ohms	N/A

Note: All values are for Zo = 50Ω

**Truth Table1: CKPWRGD\_WOL\_STOP#, OE\_96 and OE\_CPU**

CKPWRGD_WOL_STOP#	OE_96	DOT96SSC	OE_CPU	CPUCLK
0	X	X	X	X
0				
1	0	Disabled	0	Disabled
1	1	Enabled	1	Enabled

\*Assuming DOT96 Output Enable from SMBus Byte2 Bit0 sets to enable (default)

\*Assuming CPUCLK Output Enable from SMBus Byte2 Bit1 sets to enable (default)

**Truth Table 2: CKPWRGD\_WOL\_STOP# Single-ended outputs**

CKPWRGD_WOL_STOP#	Pin 16, 29, 32, 33	Pin 22	Other outputs
0	Running	Hi-Z	Low
1	Running	Running	Running

\*Assuming SMBus at default value.

**Table: CPU Spread and Frequency Selection**

CPU SS_EN	CPU FS2	CPU FS1	CPU FS0	CPU MHz	Down Spread %
Byte 0 Bit 3	Byte 0 Bit 2	Byte 0 Bit 1	Byte 0 Bit 0		
0	0	0	0	266.67	0%
0	0	0	1	133.33	0%
0	0	1	0	200.00	0%
0	0	1	1	166.67	0%
0	1	0	0	333.33	0%
0	1	0	1	100.00	0%
0	1	1	0	400.00	0%
0	1	1	1	200.00	0%
1	0	0	0	266.67	0.5%
1	0	0	1	133.33	0.5%
1	0	1	0	200.00	0.5%
1	0	1	1	166.67	0.5%
1	1	0	0	333.33	0.5%
1	1	0	1	100.00	0.5%
1	1	1	0	400.00	0.5%
1	1	1	1	200.00	0.5%

Table: DOT96 Spread and Frequency Selection Table

DOT96 SS_EN	FS3	FS2	FS1	FS0	DOT96SS MHz	Spread %	
Byte 0 bit 4	Byte 3 bit 3	Byte 3 bit 2	Byte 3 bit 1	Byte 3 bit 0			
0	0	0	0	0	96.00	0	
0	0	0	0	1	96.00	0	
0	0	0	1	0	96.00	0	
0	0	0	1	1	96.00	0	
0	0	1	0	0	96.00	0	
0	0	1	0	1	96.00	0	
0	0	1	1	0	96.00	0	
0	0	1	1	1	96.00	0	
0	1	0	0	0	96.00	0	
0	1	0	0	1	96.00	0	
0	1	0	1	0	96.00	0	
0	1	0	1	1	96.00	0	
0	1	1	0	0	96.00	0	
0	1	1	0	1	96.00	0	
0	1	1	1	0	96.00	0	
0	1	1	1	1	96.00	0	
1	0	0	0	0	96.00	+/-0.25	Center
1	0	0	0	1	96.00	+/-0.5	Center
1	0	0	1	0	96.00	+/-0.75	Center
1	0	0	1	1	96.00	+/-1.0	Center
1	0	1	0	0	96.00	-0.25	Down
1	0	1	0	1	96.00	-0.50	Down
1	0	1	1	0	96.00	-0.75	Down
1	0	1	1	1	96.00	-1.0	Down
1	1	0	0	0	96.00	-1.25	Down
1	1	0	0	1	96.00	-1.50	Down
1	1	0	1	0	96.00	-1.75	Down
1	1	0	1	1	96.00	-2.0	Down
1	1	1	0	0	96.00	-2.25	Down
1	1	1	0	1	96.00	-2.5	Down
1	1	1	1	0	96.00	-2.75	Down
1	1	1	1	1	96.00	-3.00	Down

### Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Supply Voltage	VDDxxx	-	GND - 0.5	3.3V	GND + 4.5	V	1
Maximum difference across all VDD pins	VDDdelta	-			0.5	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Junction Temperature	Tj	-			125	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

### Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V <sub>IH</sub>	3.3 V +/-5%	2		V <sub>DD</sub> + 0.3	V	1
Input Low Voltage	V <sub>IL</sub>	3.3 V +/-5%	V <sub>SS</sub> - 0.3		0.8	V	1
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>	-5		5	uA	1
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I <sub>IL2</sub>	V <sub>IN</sub> = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V <sub>IH_FS</sub>	3.3 V +/-5%	0.7		V <sub>DD</sub> + 0.3	V	1
Low Threshold Input-Low Voltage	V <sub>IL_FS</sub>	3.3 V +/-5%	V <sub>SS</sub> - 0.3		0.35	V	1
Operating Current	I <sub>DD3.3OP</sub>	all outputs driven, CPU@100M			225	mA	1
Powerdown Current	I <sub>DD3.3PD</sub>	WOL_STOP mode (default)			75	mA	1
		all diff pairs driven			30	mA	1
		all differential pairs tri-stated			8	mA	1
Input Frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V		25.00000		MHz	2
Pin Inductance	L <sub>pin</sub>				7	nH	1
Input Capacitance	C <sub>IN</sub>	Logic Inputs			4	pF	1
	C <sub>OUT</sub>	Output pin capacitance			5	pF	1
	C <sub>INX</sub>	X1 & X2 pins			5	pF	1
Clk Stabilization	T <sub>STAB</sub>	From VDD Power-Up or de-assertion of PD to 1st clock		0.5	2.5	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion		260	300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V <sub>DD</sub>		2.7		5.5	V	1
Low-level Output Voltage	V <sub>OL</sub>	@ I <sub>PULLUP</sub>			0.4	V	1
Current sinking at V <sub>OL</sub> = 0.4 V	I <sub>PULLUP</sub>		4	5		mA	1
SCLK/SDATA Clock/Data Rise Time	T <sub>RI2C</sub>	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T <sub>FI2C</sub>	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Input frequency should be measured at the REF pin and tuned to ideal 25.00MHz to meet ppm frequency accuracy on PLL outputs.

**Electrical Characteristics - CPU 0.7V Current Mode Differential Pair**

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_o = V_x$	3000			$\Omega$	1
Voltage High	VHigh	Statistical measurement on single ended signal	660	731	850	mV	1,3
Voltage Low	VLow		-150	70	150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		800	1150	mV	1
Min Voltage	Vuds		-300	8		mV	1
Crossing Voltage (abs)	Vx(abs)		250	366	550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges		16	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Average period	T <sub>period</sub>	100.00MHz nominal	9.9990	10.0000	10.0001	ns	2
		100.00MHz spread	10.0240	10.0250	10.0251	ns	2
Absolute min/max period	T <sub>absmin/max</sub>	100.00MHz nominal/spread	9.9490		10.1011	ns	1,2
Rise Time	t <sub>r</sub>	$V_{OL} = 0.175V, V_{OH} = 0.525V$	175	376	700	ps	1,4
Fall Time	t <sub>f</sub>	$V_{OH} = 0.525V, V_{OL} = 0.175V$	175	335	700	ps	1,4
Rise Time Variation	d-t <sub>r</sub>	$V_{OL} = 0.175V, V_{OH} = 0.525V$		104	125	ps	1
Fall Time Variation	d-t <sub>f</sub>	$V_{OH} = 0.525V, V_{OL} = 0.175V$		92	125	ps	1
Rise/Fall Matching	t <sub>RFM</sub>	Single-ended measurement, averaging on		12.7	20	%	1
Slew Rate	t <sub>SLEW</sub>	Differential Measurement	1	2	4	V/ns	1,5
Duty Cycle	d <sub>t3</sub>	Measurement from differential wavform	45	49.8	55	%	1
Jitter, Cycle to cycle	t <sub>jyc-cyc</sub>	Measurement from differential wavform, CPUCLK		45	50	ps	1

\*T<sub>A</sub> = 0 - 70°C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> =2pF, R<sub>S</sub>=33.2Ω, R<sub>P</sub>=49.9Ω, I<sub>REF</sub> = 475Ω

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz<sub>x</sub> is tuned to exactly 25.000MHz

<sup>3</sup>I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=50Ω.

<sup>4</sup>Rise/fall time measured on single-ended waveform per CK410 specification.

<sup>5</sup>Slew rate measured on differential waveform per CK505 specification.



**Electrical Characteristics - DOT96SS 0.7V Current Mode Differential Pair**

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Z <sub>o</sub>	V <sub>O</sub> = V <sub>x</sub>	3000			Ω	1
Voltage High	V <sub>High</sub>	Statistical measurement on single ended signal	660	725	850	mV	1,3
Voltage Low	V <sub>Low</sub>		-150	51	150	mV	1,3
Max Voltage	V <sub>ovs</sub>	Measurement on single ended signal using absolute value.		764	1150	mV	1
Min Voltage	V <sub>uds</sub>		-300	5		mV	1
Crossing Voltage (abs)	V <sub>x(abs)</sub>		250	372	550	mV	1
Crossing Voltage (var)	d-V <sub>cross</sub>	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see T <sub>period</sub> min-max values	-100	-41	100	ppm	1,2
Average period	T <sub>period</sub>	96.00MHz nominal	10.4156	10.4166	10.4176	ns	2
		96.00MHz -0.5% spread	10.4417	10.4427	10.4437	ns	2
Absolute min period	T <sub>absmin</sub>	96.00MHz nominal/-0.5% spread	10.1917		10.6937	ns	1,2
Rise Time	t <sub>r</sub>	V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V	175	361	700	ps	1,4
Fall Time	t <sub>f</sub>	V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V	175	375	700	ps	1,4
Rise Time Variation	d-t <sub>r</sub>	V <sub>OL</sub> = 0.175V, V <sub>OH</sub> = 0.525V		107	125	ps	1
Fall Time Variation	d-t <sub>f</sub>	V <sub>OH</sub> = 0.525V V <sub>OL</sub> = 0.175V		107	125	ps	1
Rise/Fall Matching	t <sub>RFM</sub>	Single-ended measurement, averaging on		15	20	%	1
Slew Rate	t <sub>SLEW</sub>	Differential Measurement	1	2	4	V/ns	1,5
Duty Cycle	d <sub>13</sub>	Measurement from differential waveform	45	51.3	55	%	1
Jitter, Cycle to cycle	t <sub>jyc-cyc</sub>	Measurement from differential waveform		54	250	ps	1

\*T<sub>A</sub> = 0 - 70°C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 2pF, R<sub>S</sub> = 33.2Ω, R<sub>P</sub> = 49.9Ω, I<sub>REF</sub> = 475Ω

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz<sub>x</sub> is tuned to exactly 25.000MHz

<sup>3</sup>I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub> = 50Ω.

<sup>4</sup>Rise/fall time measured on single-ended waveform per CK410 specification.

<sup>5</sup>Slew rate measured on differential waveform per CK505 specification.

**Electrical Characteristics - REF - 25MHz**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see T <sub>period</sub> min-max values	-50	0	50	ppm	1,2
Clock period	T <sub>period</sub>	25.00MHz output nominal	39.998	40.000	40.002	ns	2
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.4	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @ MIN = 1.0 V	-29			mA	1
		V <sub>OH</sub> @ MAX = 3.135 V			-23	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @ MIN = 1.95 V	29			mA	1
		V <sub>OL</sub> @ MAX = 0.4 V			27	mA	1
Rise Time	t <sub>r1</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	1	1.14	2	ns	1
Fall Time	t <sub>f1</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	1	1.32	2	ns	1
Skew	t <sub>sk1</sub>	V <sub>T</sub> = 1.5 V		16	500	ps	1
Duty Cycle	d <sub>f1</sub>	V <sub>T</sub> = 1.5 V	45	53.2	55	%	1
Jitter, Cycle-cycle	t <sub>jyc-cyc</sub>	V <sub>T</sub> = 1.5 V		75	200	ps	1

\*T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%, C<sub>L</sub> = 5 pF with R<sub>s</sub> as shown in the termination table (unless otherwise specified)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz<sub>x</sub> is tuned to exactly 25.000MHz

### Electrical Characteristics - RGMII - 125MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Clock period	Tperiod	125.00MHz output nominal	7.9996	8.000	8.0004	ns	1
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.4	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @ MIN = 1.0 V	-33			mA	1
		V <sub>OH</sub> @ MAX = 3.135 V			-33	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @ MIN = 1.95 V	30			mA	1
		V <sub>OL</sub> @ MAX = 0.4 V			38	mA	1
Rise Time	t <sub>r</sub>	V <sub>OL</sub> =20%×Vdd, V <sub>OH</sub> =80%×Vdd		0.66	0.75	ns	1
Fall Time	t <sub>f</sub>	V <sub>OL</sub> =20%×Vdd, V <sub>OH</sub> =80%×Vdd		0.70	0.75	ns	1
Duty Cycle	d <sub>TI</sub>	V <sub>T</sub> = 1.5 V	45	52.9	55	%	1
Group Skew	t <sub>skew_RGMII</sub>	V <sub>T</sub> = 1.5 V,		15	100	ps	1
Jitter, Long Term	t <sub>jabs</sub>	V <sub>T</sub> = 1.5 V, 10 : sec interval		141	500	ps	1
Jitter, Cycle to cycle	t <sub>j cyc-cyc</sub>	V <sub>T</sub> = 1.5 V		75	250	ps	1
Jitter, Peak	t <sub>jpeak</sub>	V <sub>T</sub> = 1.5 V		68	100	ps	1,3

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz\_x is tuned to exactly 25.000MHz

<sup>3</sup>1/2 of the peak-to-peak jitter. (Lg+ + lLg-l)/2

### Electrical Characteristics - RMII - 50MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Clock period	Tperiod	50.00MHz output nominal	19.9990	20.0000	20.001	ns	1
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.4	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @ MIN = 1.0 V	-33			mA	1
		V <sub>OH</sub> @ MAX = 3.135 V			-33	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @ MIN = 1.95 V	30			mA	1
		V <sub>OL</sub> @ MAX = 0.4 V			38	mA	1
Rise Time	t <sub>r</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	1	1.1	3	ns	1
Fall Time	t <sub>f</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	1	1.1	3	ns	1
Duty Cycle	d <sub>TI</sub>	V <sub>T</sub> = 1.5 V	35	51.5	65	%	1
Group Skew	t <sub>skew_RMII(5:0)</sub>	V <sub>T</sub> = 1.5 V, across all 6 outputs		60	200	ps	1
Jitter, Long Term	t <sub>jabs</sub>	V <sub>T</sub> = 1.5 V, 10 8sec interval		127	500	ps	1
Jitter, Peak	t <sub>jpeak</sub>	V <sub>T</sub> = 1.5 V		88	100	ps	1,3

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz\_x is tuned to exactly 25.000MHz

<sup>3</sup>1/2 of the peak-to-peak jitter. (Lg+ + lLg-l)/2

### Electrical Characteristics - 33.33MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1
Clock period	Tperiod	33.33MHz output non-spread	29.9970	30.0000	30.0030	ns	1
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.4	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @ MIN = 1.0 V	-33			mA	1
		V <sub>OH</sub> @ MAX = 3.135 V			-33	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @ MIN = 1.95 V	30			mA	1
		V <sub>OL</sub> @ MAX = 0.4 V			38	mA	1
Rise Time	t <sub>r</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	0.5	0.87	2	ns	1
Fall Time	t <sub>f</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	0.5	1.35	2	ns	1
Duty Cycle	d <sub>11</sub>	V <sub>T</sub> = 1.5 V	45	50.7	55	%	1
Jitter, Cycle to cycle	t <sub>jCyc-cyc</sub>	V <sub>T</sub> = 1.5 V		104	350	ps	1

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

### Electrical Characteristics - 32.768KHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	-79	100	ppm	1
Clock period	Tperiod	32.768KHz output nominal	30.5149	30.5180	30.5211	us	1
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4			V	1
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1 mA			0.4	V	1
Output High Current	I <sub>OH</sub>	V <sub>OH</sub> @ MIN = 1.0 V	-33			mA	1
		V <sub>OH</sub> @ MAX = 3.135 V			-33	mA	1
Output Low Current	I <sub>OL</sub>	V <sub>OL</sub> @ MIN = 1.95 V	30			mA	1
		V <sub>OL</sub> @ MAX = 0.4 V			38	mA	1
Rise Time	t <sub>r</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	1	1.39	4	ns	1
Fall Time	t <sub>f</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	1	1.6	4	ns	1
Duty Cycle	d <sub>11</sub>	V <sub>T</sub> = 1.5 V	45	49.5	55	%	1
Jitter, Cycle to cycle	t <sub>jCyc-cyc</sub>	V <sub>T</sub> = 1.5 V		220	500	ps	1

\*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

## General SMBus serial interface information for the 9FGP205

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address *D0 <sub>(H)</sub>		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
◊		ACK
◊		◊
◊		◊
◊		◊
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address *D0 <sub>(H)</sub>		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address *D1 <sub>(H)</sub>		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
ACK		Beginning Byte N
◊		◊
◊		◊
◊		◊
◊		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

\* By default, SMBADR = 0, therefore, SMBus WRITE/READ address is D0/D1. Please see SMBus Address Selection table on page 1.

**SMBus Table: CPU Frequency Select and Spread Spectrum Control Register**

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WOL_STOP_EN	Enables 25M in Power Down	RW	Disable	Enabled	1
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	-	Reserved	Reserved	RW	Reserved		0
Bit 4	-	DOT96 SS_EN	DOT96 Spread Spectrum Enable	RW	Disable	Enable	0
Bit 3	-	CPU SS_EN	CPU Spread Spectrum Enable	RW	See Table 1: CPU Frequency Selection Table		0
Bit 2	-	CPU FS2	CPU Freq Select Bit 2	RW			1
Bit 1	-	CPU FS1	CPU Freq Select Bit 1	RW			0
Bit 0	-	CPU FS0	CPU Freq Select Bit 0	RW			1

**SMBus Table: RMII Output Control Register**

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	24	RMII_5 Enable	RMII_7 Output Control	RW	Disable	Enable	1
Bit 6	25	RMII_4 Enable	RMII_6 Output Control	RW	Disable	Enable	1
Bit 5	28	RMII_3 Enable	RMII_5 Output Control	RW	Disable	Enable	1
Bit 4	29	RMII_2 Enable	RMII_4 Output Control	RW	Disable	Enable	1
Bit 3	32	RMII_1 Enable	RMII_3 Output Control	RW	Disable	Enable	1
Bit 2	33	RMII_0 Enable	RMII_2 Output Control	RW	Disable	Enable	1
Bit 1	36	RGMII_1 Enable	RGMII_1 Output Control	RW	Disable	Enable	1
Bit 0	37	RGMII_0 Enable	RGMII_0 Output Control	RW	Disable	Enable	1

**SMBus Table: DOT, CPU, 32.768KHz, 25MHz and 33.33MHz Outputs Control Register**

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	7,8	CPUCLK PD Drive Mode	Driven in power down	RW	Driven	Hi-Z	1
Bit 6	3,4	DOT96SS PD Drive Mode	Driven in power down	RW	Driven	Hi-Z	1
Bit 5	22	33.33MHz Enable	33.33MHz Output Control	RW	Disable	Enable	1
Bit 4	17	25MHz_1 Enable	25MHz_1 Output Control	RW	Disable	Enable	1
Bit 3	16	25MHz_0 Enable	25MHz_0 Output Control	RW	Disable	Enable	1
Bit 2	13	32.768kHz Enable	32.768KHz Output Control	RW	Disable	Enable	1
Bit 1	6	CPUCLK Enable	CPUCLK Output Control	RW	Disable	Enable	1
Bit 0	5	DOT96SS Enable	DOT96SS Output Control	RW	Disable	Enable	1

**SMBus Table: DOT96 Frequency Select and Spread Spectrum Control Register**

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	24	RMII_5 WOL_STOP	RMII_5 runs in power down	RW	Off	Runs	0
Bit 6	25	RMII_4 WOL_STOP	RMII_4 runs in power down	RW	Off	Runs	0
Bit 5	28	RMII_3 WOL_STOP	RMII_3 runs in power down	RW	Off	Runs	0
Bit 4	29	RMII_2 WOL_STOP	RMII_2 runs in power down	RW	Off	Runs	1
Bit 3	-	DOT96SS FS3	DOT96 Freq Select Bit 3	RW	See Table 2: DOT Frequency Selection Table		0
Bit 2	-	DOT96SS FS2	DOT96 Freq Select Bit 2	RW			0
Bit 1	-	DOT96SS FS1	DOT96 Freq Select Bit 1	RW			0
Bit 0	-	DOT96SS FS0	DOT96 Freq Select Bit 0	RW			0

**SMBus Table: RMII Strength Control Register**

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	24	RMII_5 Str	RMII_5 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 6	25	RMII_4 Str	RMII_4 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 5	28	RMII_3 Str	RMII_3 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 4	29	RMII_2 Str	RMII_2 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 3	32	RMII_1 Str	RMII_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 2	33	RMII_0 Str	RMII_0 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 1	32	RMII_1 WOL_STOP	RMII_1 runs in power down	RW	Off	Runs	1
Bit 0	33	RMII_0 WOL_STOP	RMII_0 runs in power down	RW	Off	Runs	1

SMBus Table: 32.768KHz, 25Mhz and 33.33MHz Strength Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	22	33.33MHz Str	33.33MHz Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 4	17	25MHz_1 Str	25MHz_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 3	16	25MHz_0 Str	25MHz_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 2	13	32.768kHz Str	32.768kHz Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 1	17	25MHz_1_WOL_STOP	25MHz_1 runs in power down	RW	Off	Runs	0
Bit 0	16	25MHz_0_WOL_STOP	25MHz_0 runs in power down	RW	Off	Runs	1

SMBus Table: Vendor & Revision ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	A rev = 0000 B rev = 0001		X
Bit 6	-	RID2		R			X
Bit 5	-	RID1		R			X
Bit 4	-	RID0		R			X
Bit 3	-	VID3	VENDOR ID	R	ICS/IDT = 0001		0
Bit 2	-	VID2		R			0
Bit 1	-	VID1		R			0
Bit 0	-	VID0		R			1

SMBus Table: Device ID

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)	Device ID	R	Reserved		0
Bit 6	-	Device ID 6		R	Reserved		0
Bit 5	-	Device ID 5		R	Reserved		1
Bit 4	-	Device ID 4		R	Reserved		0
Bit 3	-	Device ID 3		R	Reserved		0
Bit 2	-	Device ID 2		R	Reserved		1
Bit 1	-	Device ID 1		R	Reserved		0
Bit 0	-	Device ID 0 (LSB)		R	Reserved		1

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	0
Bit 1	-	BC1		RW	-	-	0
Bit 0	-	BC0		RW	-	-	1

SMBus Table: Reserved

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

SMBus Table: PLLs M/N Programming Enable Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLLs M/N Programming Enable	RW	Disable	Enable	0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $25 \times [NDiv(9:0)+8] / [MDiv(5:0)+2]$		X
Bit 6	-	N Div 9	N Divider Prog bit 9	RW			
Bit 5	-	M Div5	M Divider Programming bits	RW			
Bit 4	-	M Div4		RW			
Bit 3	-	M Div3		RW			
Bit 2	-	M Div2		RW			
Bit 1	-	M Div1		RW			
Bit 0	-	M Div0		RW			

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = $25 \times [NDiv(9:0)+8] / [MDiv(5:0)+2]$		X
Bit 6	-	N Div6		RW			
Bit 5	-	N Div5		RW			
Bit 4	-	N Div4		RW			
Bit 3	-	N Div3		RW			
Bit 2	-	N Div2		RW			
Bit 1	-	N Div1		RW			
Bit 0	-	N Div0		RW			

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			
Bit 5	-	SSP5		RW			
Bit 4	-	SSP4		RW			
Bit 3	-	SSP3		RW			
Bit 2	-	SSP2		RW			
Bit 1	-	SSP1		RW			
Bit 0	-	SSP0		RW			

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			Reserved				0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			
Bit 4	-	SSP12		RW			
Bit 3	-	SSP11		RW			
Bit 2	-	SSP10		RW			
Bit 1	-	SSP9		RW			
Bit 0	-	SSP8		RW			

SMBus Table: DOT PLL VCO Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = $25 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			
Bit 5	-	M Div5	M Divider Programming bits	RW			
Bit 4	-	M Div4		RW			
Bit 3	-	M Div3		RW			
Bit 2	-	M Div2		RW			
Bit 1	-	M Div1		RW			
Bit 0	-	M Div0		RW			

SMBus Table: DOT PLL VCO Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divider in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = $25 \times [\text{NDiv}(9:0)+8] / [\text{MDiv}(5:0)+2]$		X
Bit 6	-	N Div6		RW			
Bit 5	-	N Div5		RW			
Bit 4	-	N Div4		RW			
Bit 3	-	N Div3		RW			
Bit 2	-	N Div2		RW			
Bit 1	-	N Div1		RW			
Bit 0	-	N Div0		RW			

SMBus Table: DOT PLL Spread Spectrum Control Register

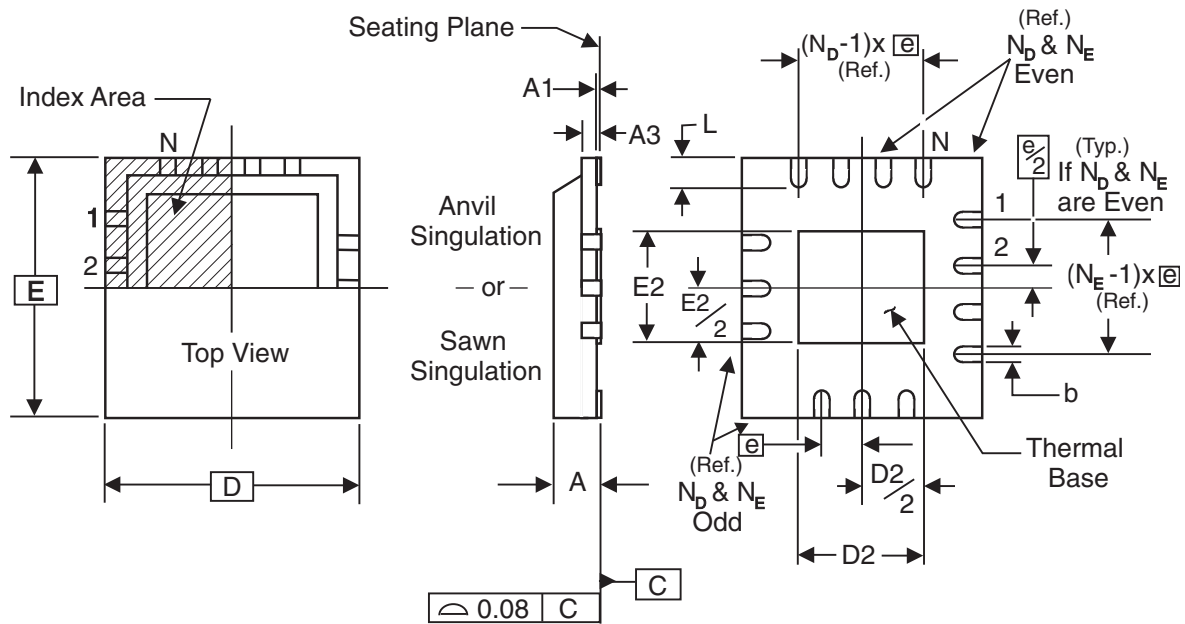
Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			
Bit 5	-	SSP5		RW			
Bit 4	-	SSP4		RW			
Bit 3	-	SSP3		RW			
Bit 2	-	SSP2		RW			
Bit 1	-	SSP1		RW			
Bit 0	-	SSP0		RW			

SMBus Table: DOT PLL Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		Reserved				0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread percentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			
Bit 4	-	SSP12		RW			
Bit 3	-	SSP11		RW			
Bit 2	-	SSP10		RW			
Bit 1	-	SSP9		RW			
Bit 0	-	SSP8		RW			

Bytes 19:21 are reserved.





**THERMALLY ENHANCED, VERY THIN, FINE PITCH  
QUAD FLAT / NO LEAD PLASTIC PACKAGE**

**DIMENSIONS**

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	

**DIMENSIONS** (JEDEC reference only) (IDT package)

SYMBOL	VJJD-2 / -5	40L TOLERANCE
N	40	40
$N_D$	10	10
$N_E$	10	10
D x E BASIC	6.00 x 6.00	6.00 x 6.00
D2 MIN. / MAX.	1.75 / 4.80	2.75 / 3.0
E2 MIN. / MAX.	1.75 / 4.80	2.75 / 3.0
L MIN. / MAX.	0.30 / 0.50	0.3 / 0.5

**Ordering Information**

Part / Order Number	Shipping Packaging	Package	Temperature
9FGP205AKLF	Trays	40-pin MLF	0 to +70° C
9FGP205AKLFT	Tape and Reel	40-pin MLF	0 to +70° C

“LF” to the suffix are the Pb-Free configuration and are RoHS compliant.  
“A” is the device revision designer (will not correlate with the datasheet revision).

**Revision History**

Rev.	Issue Date	Who	Description	Page #
0.1	4/13/2009	RDW	Initial Release	-
0.2	4/30/2010	RDW	1. Changed name of Pin 40 to CKPWRGD_WOL_STOP# to update description. No change in functionality. 2. Added control bits to Byte 3, 4, and 5 to select WOL_STOP# functionality for the 25M REF outputs and the 50M RMII outputs. Note default settings. 3. Updated Table 1 (combined with Table 2) 4. Changed Table 2 to reflect WOL_STOP function for pins 16, 29, 32, 33. 5. Added WOL_STOP entry for power down current. 6. Updated/corrected block diagram by removing OE_RMII pins.	
0.3	5/3/2010	RDW	1. Corrected error in Truth Table 2, added separate column for Pin 22.	5
0.4	5/14/2010	RDW	1. CPU and DOT 96 default power down mode changed from driven to Hi-Z to support WOL_STOP# mode. Termination circuit will give Low/Low on those outputs in Power Down. Byte 2, but 7 and 6 default changed to 1. 2. Corrected byte 7 to be Read Only.	13, 14

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